NETWORK-ON-CHIP FAULT DETECTION AND ROUTER SELF-TEST

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requirements for the award of the degree of
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Dedicated, in thankful appreciation for support and encouragement to my beloved wife Nabilah, my daughter Aleesya, my parents, families and friends.

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ABSTRACT

Network-on-Chip (NoC) router is an entity that facilitates communication between subsystem or IP cores on an integrated circuit. Faults such as permanent fault, transient fault and random fault are commonly observed on a NoC router. They may severely impact the functionality of an NoC router if not handled appropriately. This project proposes a mechanism to identify error and perform self-testing in NOC router by enhancing the Register Transfer Level (RTL) design of CONNECT NoC Baseline Router with error detection mechanism, as well as devising a built in self-test mode for NOC router. Both proposed error detection mechanism and built in self-test mode have been successfully implemented using System Verilog. The work presented in this project shows possible enhancement to NoC router architecture to detect erroneous packets. NoC router is able to detect faults through proposed error dection tecchniques. This allows router self-test in order to sustain the functionality of a system in the presence of faults. Simulation results show that additional logics do not affect NoC router performance.

ABSTRAK

Rangkaian-pada-Chip (NoC) router adalah entiti yang memudahkan komunikasi antara subsistem atau IP teras pada litar bersepadu. Kerosakan seperti kerosakan kekal, sementara dan rawak biasanya terjadinya pada router NoC. Kerosakan ini boleh memberi kesan teruk kepada fungsi sesuatu router NOC jika tidak ditangani dengan sewajarnya. Projek ini mencadangkan satu mekanisme untuk mengenal pasti kesilapan dan melakukan ujian diri dalam NoC router dengan meningkatkan Tahap Daftar Pemindahan (RTL) reka bentuk NoC Router dengan mekanisme pengesanan ralat, serta merangka terbina dalam mod ujian diri untuk NoC router. Kedua-dua mekanisme pengesanan ralat dicadangkan dan dibina dalam mod ujian diri telah berjaya dilaksanakan dengan menggunakan Sistem Verilog. Kerja-kerja yang dibentangkan dalam projek ini menunjukkan peningkatan mungkin untuk seni bina router NoC untuk mengesan paket salah. NoC router mampu mengesan kesalahan melalui dicadangkan tecchniques ralat dection. Ini membolehkan router sendiri ujian-bagi mengekalkan fungsi sistem yang di hadapan-dosa. Keputusan simulasi menunjukkan bahawa Logika tambahan tidak menjejaskan prestasi router NoC.